Remarks:

In the Office Action mailed on February 2, 2009, the Examiner rejected claims 1-41. Applicants amend claims 11-13, 23, 25-31 and 38-41 herein. Claim 24 has been cancelled herein.. Claims 1-23 and 25-41 are pending in the application.

The Claims

35 USC 101

Claims 13, 23-31, 38-39 and 41were rejected under 35 USC 101 because the claimed invention is directed to non-statutory subject matter.

The Examiner asserted that "Claim 13, as claimed, is merely drawn to non-statutory descriptive material since the claim is of a 'computer program'." Office Action, Page 2, Lines 9-10. Claims 23-31, 38-39, and 41 were rejected as inheriting the alleged defect.

Applicants have amended Claim 13 to direct it to a computer readable storage medium with program instructions to cause a microprocessor to perform acts such as defining and designating areas in physical memory. As such, Claim 13 is directed to a particular apparatus (the computer readable storage medium) and is therefore directed to statutory subject matter.

Accordingly, Applicants respectfully request withdrawal of the rejection under 35 USC 101 and the allowance of Claims 13, 23, 25-31, 38-39 and 41.

35 USC 112, second paragraph

Claims 11, 12, 40 and 41 were rejected under 35 USC 112, first paragraph as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s) at the time the application was filed, had possession of the claimed invention.

While Applicants contend that the previous version of Claim 11, 12, 40, and 41 were supported adequately by the specification, Applicants have amended these claims to more clearly recite the subject matter of the invention. In these

amendments, Claim 11 being a good example, "requires an erase operation" has been changed to "cannot be achieved by not writing to the active physical area or by performing bit programming operations", and "designating the active area to be an unwritten physical area in the mirror memory" has been changed to "designating a new active physical area." These recitations are supported by the specification, for example, in paragraphs [0042] for "not written to", [0043] for "bit programming". Designation of an active area (by setting a bit) is, for example, described in paragraph [0037].

Accordingly, Applicants respectfully request withdrawal of the rejection under 35 USC 112, second paragraph, and the allowance of Claims 1-31.

35 USC 102

Claims 1-2, 11, 13, 23, 32-35 and 38-41 stand rejected under 35 U.S.C. 102(b) as being anticipated by Ban (WO 94/20906 hereinafter "Ban").

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Manual of Patent Examining Procedure (Eighth) § 2131 (2005) (quoting Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631 (Fed. Cir. 1987)). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Id.* (quoting Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236 (Fed. Cir. 1989)). This standard cannot be met with Ban.

In response to the last office action, Applicants submitted a lengthy argument illustrating that Ban does not anticipate Applicants' invention (Response, January 9, 2009). That response is incorporated here in its entirety.

Applicants wish to highlight a few important points.

First, the notion of a logical area versus a physical area. In computer science a *logical* entity, be it a logical unit, logical address, logical memory area, is a manner in which the *logic*, i.e., the programs, for example, the operating system, views these entities. A logical address then, is an address used by a program to address some memory location. A memory area is some portion of a memory. Thus, a *logical* memory area is a collection of logical addresses that are grouped together. Figure 2

of Applicants' application illustrates the concept well. When a program is writing to the memory in operations (E1) … (En), these operations address the *logical area* ZL.

The converse of *logical* is *physical*. The *physical* entities are the actual physical electronic devices located in a computer. Examples, include, physical disks, physical memory, physical addresses. For example, *physical memory* would be the actual electronic circuit that allows for data storage. The *physical memory* has its own addressing scheme separate from the logical addressing scheme. However, whenever a program, using the logical addressing scheme to access a memory location, the logical address of that memory location is translated into a corresponding physical address. Similarly, a *logical area* would correspond to a *physical* area.

In applicants' technology, the *logical area ZL* that may be addressed by a program is mapped into multiple that may be addressed by a program is mapped into multiple *physical* areas ZP1 … ZPn. These are mirror areas, by which the applicants mean that these multiple physical areas are mapped to the same logical area. They mirror each other.

Ban fails to teach or suggest "defining mirror areas"

Applicants claim "defining a mirror area in the flash type memory divided into at least two physical areas" (Claim 1). For that proposition, the Examiner offers "block, areas, units or zones: page 2, line 21-page 3, line 15, page 3, lines 1-2". Office Action, Page 4, Lines 6-7. Let us consider what is actually taught there:

> "The flash memory physical locations are organized as an array of bytes. Each of the bytes in the array is assigned a number of address by means of which the byte is physically accessible, referred to herein as the physical address space. Each of the bytes in the array has a second address, called the virtual address space. A table, called a virtual map, converts virtual addresses to physical addresses. Here it should be noted, the virtual address space is not necessarily the same size as the physical address space." (Ban, page 2, Line 21-29).

Thus, all that this first section of the cited passage discusses is virtual addressing and the notion of mapping virtual addresses to physical addresses. There is no notion of defining a mirror area in the memory divided into at least two physical areas. Let's examine the next section of the cited passage:

> "A contiguous, fixed-length group of physical byte addresses from (sic) a block. For example, assuming a block size of 512 bytes, a byte with a physical address of 256211 is bytes number 211 in block 500 (256211 : 51 = 500 + 211). One or more physically contiguous flash memory areas (called zones) that can be physically erased using suitable prior art flash memory technology comprise a unit and each unit contains an integral number of blocks." (Ban, page 3, Lines 1-7)

This section defines a hierarchical relationship in the addressing of memory locations in the physical address space. An address addresses a byte, a block addresses 512 bytes, and blocks are arranged in Zones that may be erased together. Again, absolutely nothing about mirror areas.

Next Ban teaches:

> "The virtual memory map is a table in which the first entry belongs to virtual block 0, the second to virtual block 1, and so on. Associated in the table with each virtual block address there is a corresponding physical address. In a read from the flash memory operation, a computer generated address is decoded as a virtual block address and a byte location within the block. The virtual memory map is used to convert the virtual block address to a physical block address; the byte location is the same in the virtual address space and the physical address space." (Ban, Page 3, Lines 8-15)

This section of Ban is simply a disclosure of a memory map mapping virtual memory blocks to physical block and to state that the byte location within a block, virtual or physical, is the same. Thus, this also is not a teaching of mirror areas.

The three paragraphs cited by the Examiner for the teaching of "defining a mirror area in the flash type memory divided into at least two physical areas" teach that virtual addresses are mapped to physical addresses, that there is a hierarchical organization in addressing by organizing memory as blocks and zones, and that

virtual blocks are mapped to physical blocks. None of that is a teaching or a suggestion of defining mirror areas.

Ban fails to teach or suggest "at least two [physical areas] designated to correspond to a same logical area"

The first element of Claim 1 continues with "each [physical area] designated to correspond to a same logical area for storing content written to the logical area." Recall that in the concept of logical and physical addressing access by a program is to a logical address and that address is translated to a physical address. Thus, what this recitation deals with is that the multiple mirror areas each correspond to a same logical area for storing content written to the logical area. This is a deviation from what is typically the case in virtual memory systems such as Ban, for example. In such systems, including Ban, there is a one-to-one mapping between the virtual address and the corresponding physical address. Consider, for example, "[t]he virtual memory map is used to convert the virtual block address to a physical block address; the byte location is the same in the virtual address space and the physical address space" (Ban, Page 3, Lines 13-15). One would expect that if the physical address is organized so that the virtual block address corresponded to multiple mirror areas in the physical space that there would be some indication in Ban to indicate which of those multiple mirror areas a given access to a virtual block cause. However, Ban nowhere mentions how to select one of a plurality of areas to access, because there is no mapping of one virtual block (or any other memory area) to corresponding multiple blocks in the physical memory.

For the claimed proposition that "each [physical area] designated to correspond to a same logical area for storing content written to the logical area" the examiner recites as follows:

> "fixed-length group of physical byte addresses form a logical block, page 3, lines 1-2; one or more physically contiguous flash memory areas or zones comprise a number of blocks, page 3, lines 4-7; therefore the physical byte addresses are associated with logical blocks, zones and units, FIG. 2, 3, & 7; Furthermore, there are a plurality of Logical areas associated with a

fixed-length group of physical byte addresses: FIG. 3, 4, 7 and page 2 line 21-page 3, line 15" (Office Action, Page 4, Lines 11-18).

What Ban actually states in Page3, lines 1-2 is that "[a] contiguous, fixed-length group of physical byte addresses from (sic) a block." There is no mention in that sentence of "logical." Ban is merely stating that he defines an addressing structure called a block and he is organizing contiguous addresses (e.g., 512 bytes) as a block. A block is just a convenient notion for designating a sequence of contiguous addresses.

That aside, the Examiner's reasoning is very flawed in its aim to show that Ban allegedly teaches "each [physical area] designated to correspond to a same logical area for storing content written to the logical area." The examiner states that "therefore the physical byte addresses are associated with logical blocks, zones and units." Be that as it may. That only states that given a particular physical address that address corresponds to a logical block, a zone and a unit (and of course a logical address within that block even if the examiner left that out). For example that would mean that given one physical address that physical address corresponds to a zone, a block, a unit, and an address. However, it does not mean that a logical address (or more specifically in the claim language, a *logical area*) corresponds to at least two physical addresses, each in a distinct physical area.

The examiner states "Furthermore, there are a plurality of logical areas associated with a fixed-length group of physical addresses." That may be true. However, Ban never states that and more importantly for this context, that is not what applicants are claiming. Applicants claim "each [physical area] designated to correspond to a same logical area for storing content written to the logical area," i.e., that one logical area corresponds to multiple (at least two) physical areas. Thus, while the Examiner has misread Ban, the Examiner's conclusion of what Ban teaches is not what is being claimed, and Ban also fails to teach or suggest "each [physical area] designated to correspond to a same logical area for storing content written to the logical area."

Ban fails to teach or suggest "designating one of the at least two physical areas as being an active physical area"

From the foregoing it must be abundantly clear that Ban fails to teach or suggest "designating one of the at least two physical areas as being an active physical area." A claim must be considered as a whole. Therefore, when analyzing the meaning of an element, the other elements cannot be ignored. Thus, while applicants have amended claim 1 to now specifically state that this element refers to designating *one of the at least two* physical areas, it must be interpreted to mean that this is a selection of one of the at least two physical areas that make up the mirror area in which each of the at least two physical areas correspond to the same logical area. This designation, then, is a selection to indicate which one of a plurality is to be *the one* to which accesses are to be made. Because Ban does not teach or suggest this type of mirroring in which multiple physical areas are made to correspond to one and the same logical area, there is no need in Ban to designate one of these areas for access and, not surprisingly, Ban does not teach or suggest doing so.

The Examiner has not offered any citation into Ban (or any other reference) for a purported teaching of the designation of one of the at least two physical areas as the active area. Thus, Applicants posit that this is in of itself a failure to provide a rational basis for the rejection.

Ban fails to teach or suggest "during a write to said logical area, programming the content of said logical area into the active physical area"

A claim must be considered as a whole. Therefore, when analyzing the meaning of an element, the other elements cannot be ignored. Thus, when applicants claim "during a write to said logical area, programming the content of said logical area into the active physical area," that element refers to writing into the active physical area in the set of at least two physical areas corresponding to a same logical area wherein the active physical area is the one physical area active for access. Because Ban fails to teach or suggest organizing physical memory into a mirror area having at least two physical areas corresponding to the same logical area, there is not in Ban a designated active area and, consequently, it is impossible in Ban to write into

the active area when *the active area* means the one of at least two physical areas designated for access. Therefore, Ban fails to teach or suggest this element also.

The Examiner offers the abstract of Ban for the proposition "during a write". Applicants concede that indeed Ban does teach writing into memory. For the remainder of the element the Examiner offers the following:

> "flash memory system which 'allows data to be continuously written to unwritten physical address locations,' abstract; data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming. page 1, lines 26-29; page 7, lines 1 – page 9, line 22, and page 13, claim 1" (Office Action, Page 4, line 20 – Page 5, Line 4.

Applicants concede that writing to flash memories typically can only be done when the flash memory has previously not been written to (unless the write operation leaves the previously written bits untouched). In applicants' novel and non-obvious invention that restriction is what is being addressed by having a mirror memory with multiple physical areas corresponding to the same logical area. The applicants designate one of these areas to be the one to which writes are to occur (the active area). Ban merely writes to *the* physical memory corresponding to the virtual memory location being addressed. Of course, if it is a flash memory that memory location cannot have been previously written to without first being erased. However, that does not equate writing into the active area that has been designated as such from a sequence of physical memory areas that each correspond to the same logical area. Accordingly, the Examiner's reasoning for why Ban allegedly teaches "during a write to said logical area, programming the content of said logical area into the active physical area" is incomplete because all it stands for is writing into unwritten flash memory but not writing into an active area.

As noted, for a claim to be anticipated by a reference, all elements of the claim must be taught by that reference. In the present case, none of the elements are taught or suggested by the reference. Accordingly, Claim 1 is not anticipated by Ban.

Claims 11and 13 recite similar limitations to those set forth in Claim 1 and are patentable over Ban for at least the same reasons as given in support of Claim 1.

35 USC 103

Claims 3, 7-8, 18, 24, and 28-29 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1-2, 13, and 23 and in further view of Assar et al. (WO 95/10083) hereinafter Assar. Claims 4 and 25 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1 and 13 and further in view of Mennecart (WO 01/88926 A1) hereinafter Mennecart. Claims 5 and 26 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 2 and 13 and further in view of Hazen et al (WO 99/35650) hereinafter Hazen. Claims 6 and 27 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claims 5 and 26 and in view of Lipovski (US 5,758,148) hereinafter Lipovski. Claims 9-10 and 30-31 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1-2 and 13 and further in view of Kuo (US 4,763,305) hereinafter Kuo. Claim 12, 36 and 37 are rejected under 35 U.S.C.103 (a) as unpatentable over Ban and further in view of Robinson et al (US 5,375,222). Claims 14-17 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claims 5 and 6 and further in view of Assar. Claims 19-20 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claim 5 and 6 and further in view of Kuo. Claims 21and 22 are rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Assar as applied to claim 7 and further in view of Kuo.

As discussed herein above, Claims 1, 11, and 13 are patentable over Ban. Claim 12 recites analogous limitations to those recited in Claim 1. Therefore, Claim 12 is patentable over Ban for all the same reasons given in support of Claim 1.

Assar, Mennecart, Hazen, Lipovski, and Kuo are cited by the Examiner for propositions other than that argued hereinabove. None of those references teach or suggest "associating at least two physical areas of said memory, called mirror areas, with a same and unique logical area for storing a content; designating one of the physical areas as being an active physical area; and during a write to said logical area, programming the content of said logical area into the active physical area" (Claim 1

and analogous in the other independent claims). Therefore, Claim 1 and the other independent claims are patentable over these references taken singly, or in any combination including or not including Ban.

Therefore, because all the dependent claims depend from the independent claims, incorporate all the limitations thereof and provide further unique and non-obvious combinations, the dependent claims are patentable for, at least, the reasons given in support of the independent claims. (Applicants reserve the right to argue the independent patentability of the various dependent claims in response to any further rejection of these claims)

The application is now deemed to be in condition for allowance and notice to that effect is solicited.

CONCLUSION

It is submitted that all of the claims now in the application are allowable. Applicants respectfully request consideration of the application and claims and its early allowance. If the Examiner believes that the prosecution of the application would be facilitated by a telephonic interview, Applicants invite the Examiner to contact the undersigned at the number given below.

Applicants respectfully request that a timely Notice of Allowance be issued in this application.

Respectfully submitted,

Date: June 1, 2009

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